SPEC

11. In the example embodiment, the lower yield strength solder material, a AgSn solder in the example, acts as the die bump. The solder is electroplated on the die to form the die bumps 10. The copper bumps 8 on the substrate may be copper columns or studs, as needed. They are electroplated on the substrate lands or pads to provide standoffs, and to lower the resistance of the interconnect. If copper columns are not needed for performance, a solder with a melting temperature higher than the melting temperature of the solder on the die could be electroplated on the substrate for stand-off.

The present invention addresses the problem of ILD delamination under the die bumps during temperature cycling of the package by lowering the yield strength of the die bump material in relation to the copper or other conductive material of the contact member/stand-off on the substrate. This change has been found to help ILD integrity. Lowering the yield strength of the die bump material reduces the stresses transferred to the die (simplistically, the bump deforms inelastically absorbing energy). More specifically, crystal structure correlations, and measurements indicate that the yield strength of the electroplated copper used for the die bumps in the conventional interconnect scheme of Figs. 1-3, is in the 350-450 MPa range, making the bump extremely stiff. During temperature excursions (before and after die-attach), this stiff bump induces a significant 20

stress after die-attach in the case of having the copper bump on the substrate is about half that of the current case where the copper bump is on the die. This difference is due to the large yield strength of electroplated copper (400 MPa) as opposed to the much lower yield strength for the AgSn solder (around 40 MPa at room temperature). The lower yield strength of the solder die bump of the present invention will relieve some of the stress (by undergoing local plastic deformation), without transferring it to the die ILD layers. The difference will be even more in the case of temperature cycling, where the cooling cycle will make the residual stress at the bump edge (shown in Fig. 6) positive, increasing the stress for the case where the copper bump is on the die. To put the 50% reduction in ILD stresses with the AgSn/Cu/organic material substrate (OLGA) combination of the invention (in the right side of Fig. 7) in perspective, the reduction in ILD stresses by going to a ceramic substrate (Cu/AgSn/ceramic) with 6.5 ppm/°C CTE is only about 20%. Note, that even though the substrate in the conventional package of Figs. 1-3 and the substrate in the package of the present invention illustrated in Figs. 8-10 is a low cost organic substrate, this method can be applied to other common substrate materials like ceramic. However, the plastic and organic substrate materials have relatively high CTEs, along the order of 17 ppm/°C. The relatively larger CTE mismatch in packages

– yielding strength